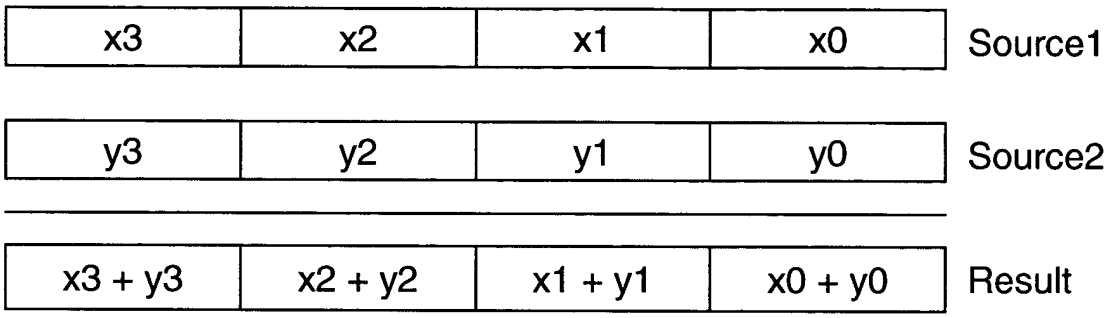
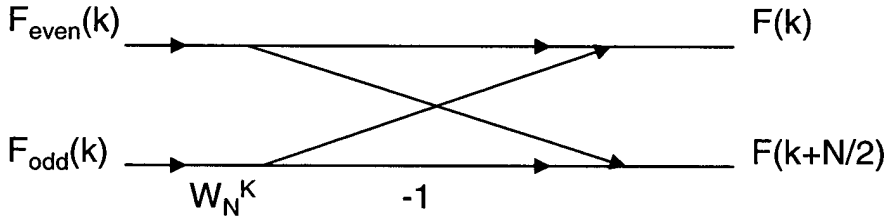


FIG. 1
(PRIOR ART)



$$F(k) = (1/2)\bullet(F_{even}(k) + F_{odd}(k)\bullet W_N^K)$$

$$F(k+N/2) = (1/2)\bullet(F_{even}(k) - F_{odd}(k)\bullet W_N^K)$$

FIG. 2a

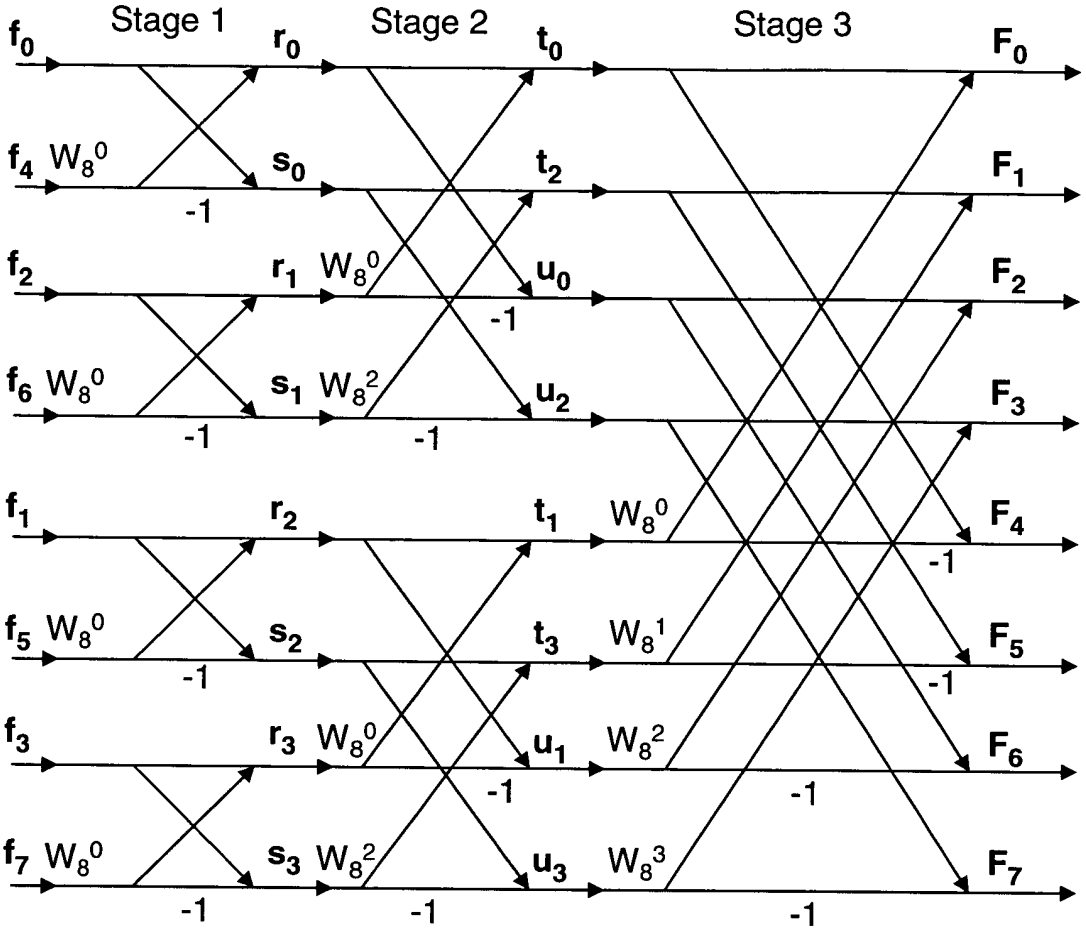

Stage 1
Stage 2
Stage 3
f0
f4 W8^0
f2
f6 W8^0
f1
f5 W8^0
f3
f7 W8^0
r0
s0
r1 W8^0
s1 W8^2
r2
s2
r3 W8^0
s3 W8^2
t0
t2
u0
u2
t1 W8^0
t3 W8^1
u1 W8^2
u3 W8^3
F0
F1
F2
F3
F4
F5
F6
F7
-1

FIG. 2b

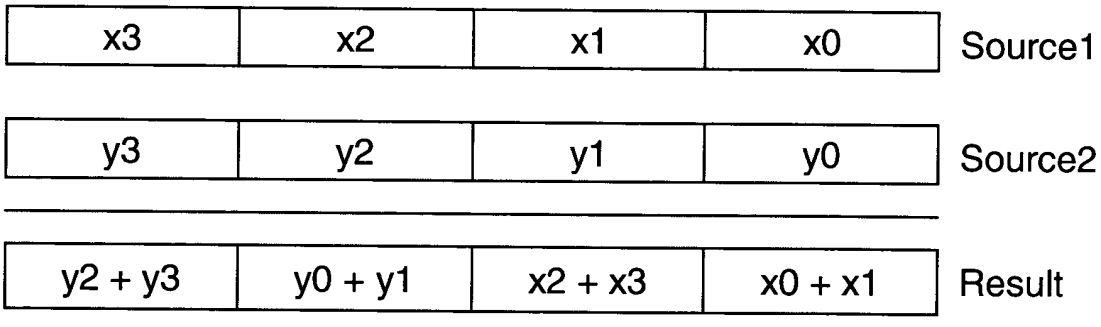

x3
x2
x1
x0
Source1
y3
y2
y1
y0
Source2
y2 + y3
y0 + y1
x2 + x3
x0 + x1
Result

FIG. 3a

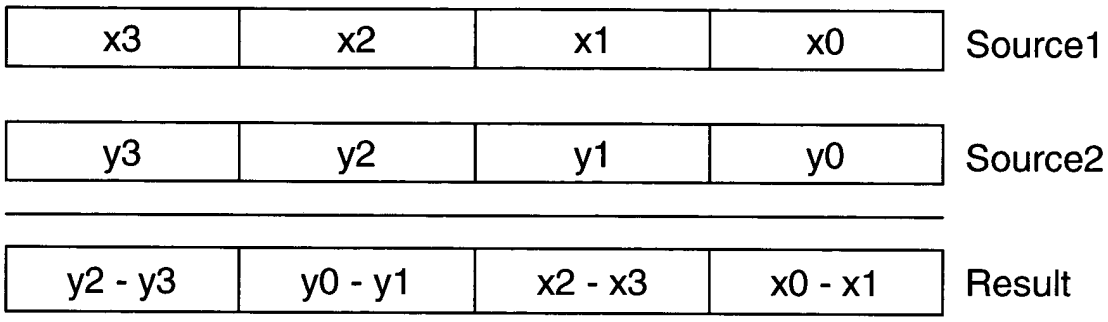


FIG. 3b

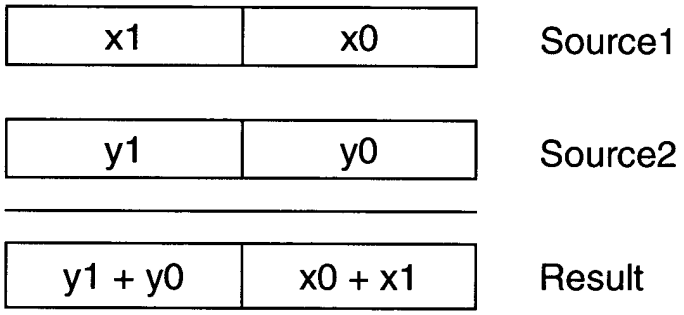


FIG. 3c

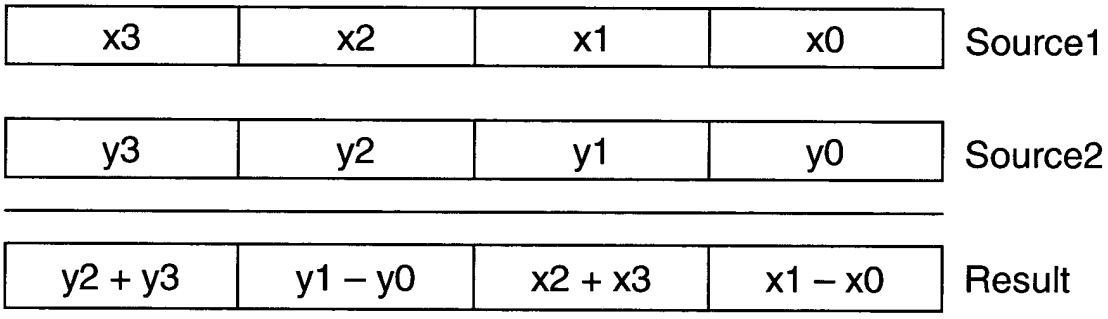


FIG. 3d

MULTIPLY – STAGE1 INPUTS1, WEIGHT1

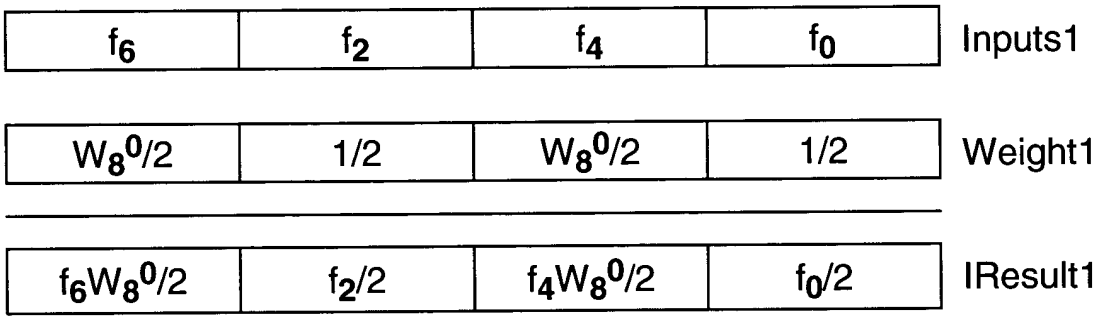


FIG. 4a

MULTIPLY – STAGE1 INPUTS2, WEIGHT1

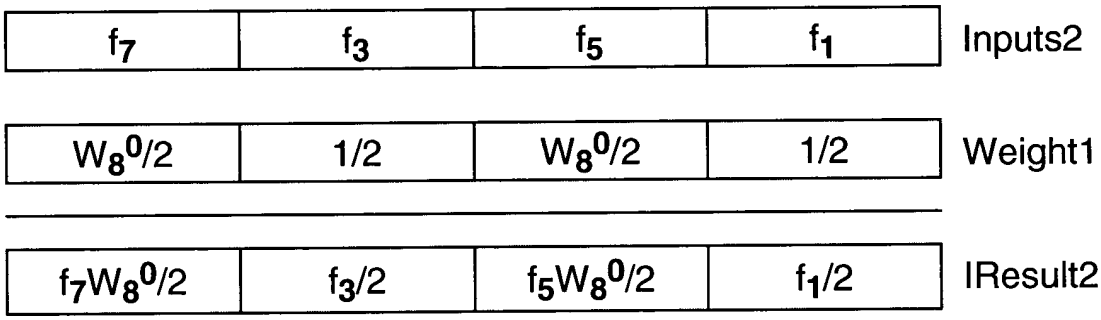


FIG. 4b

INTRA-ADD: DATA ELEMENTS OF IRESUT1, IRESULT2

$f_6W_8^0/2$	$f_2/2$	$f_4W_8^0/2$	$f_0/2$	IResult1
$f_7W_8^0/2$	$f_3/2$	$f_5W_8^0/2$	$f_1/2$	IResult2
$(f_3+f_7W_8^0)/2$	$(f_1+f_5W_8^0)/2$	$(f_2+f_6W_8^0)/2$	$(f_0+f_4W_8^0)/2$	R3-R0

FIG. 4c

INTRA-SUBTRACT: DATA ELEMENTS OF IRESUT1, IRESULT2

$f_6W_8^0/2$	$f_2/2$	$f_4W_8^0/2$	$f_0/2$	IResult1
$f_7W_8^0/2$	$f_3/2$	$f_5W_8^0/2$	$f_1/2$	IResult2
$(f_3-f_7W_8^0)/2$	$(f_1-f_5W_8^0)/2$	$(f_2-f_6W_8^0)/2$	$(f_0-f_4W_8^0)/2$	S3-S0

FIG. 4d

MULTIPLY – STAGE2 R3-R0, WEIGHT1

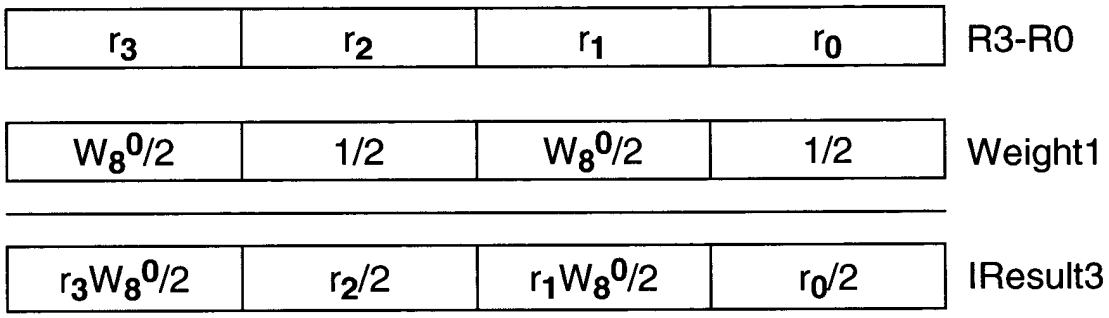


FIG. 4e

MULTIPLY – STAGE2 S3-S0, WEIGHT2

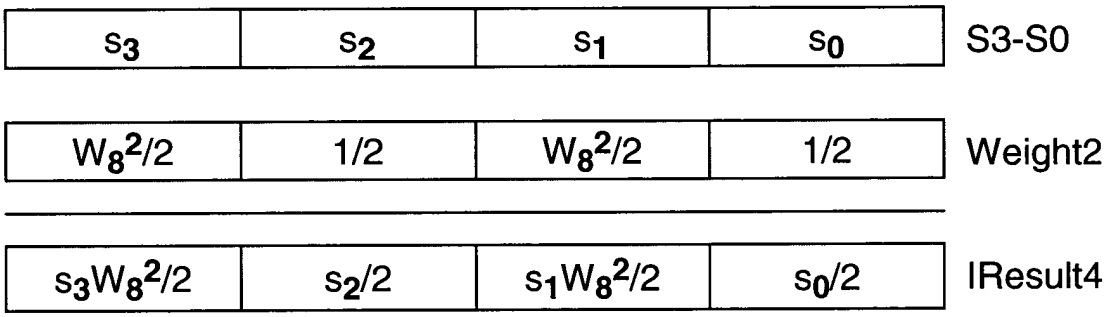


FIG. 4f

INTRA-ADD: DATA ELEMENTS OF IRESUT3, IRESULT4

$r_3W_8^0/2$	$r_2/2$	$r_1W_8^0/2$	$r_0/2$	IResult3
$s_3W_8^2/2$	$s_2/2$	$s_1W_8^2/2$	$s_0/2$	IResult4
$(s_2+s_3W_8^2)/2$	$(s_0+s_1W_8^2)/2$	$(r_2+r_3W_8^0)/2$	$(r_0+r_1W_8^0)/2$	T3-T0

FIG. 4g

INTRA-SUBTRACT: DATA ELEMENTS OF IRESUT3, IRESULT4

$r_3W_8^0/2$	$r_2/2$	$r_1W_8^0/2$	$r_0/2$	IResult3
$s_3W_8^2/2$	$s_2/2$	$s_1W_8^2/2$	$s_0/2$	IResult4
$(s_2-s_3W_8^2)/2$	$(s_0-s_1W_8^2)/2$	$(r_2-r_3W_8^0)/2$	$(r_0-r_1W_8^0)/2$	U3-U0

FIG. 4h

MULTIPLY – STAGE3 T3-T0, WEIGHT3

t_3	t_2	t_1	t_0	T3-T0
$W_8^1/2$	1/2	$W_8^0/2$	1/2	Weight3
$t_3W_8^1/2$	$t_2/2$	$t_1W_8^0/2$	$t_0/2$	IResult5

FIG. 4i

MULTIPLY – STAGE3 U3-U0, WEIGHT4

u_3	u_2	u_1	u_0	U3-U0
$W_8^3/2$	1/2	$W_8^2/2$	1/2	Weight4
$u_3W_8^3/2$	$u_2/2$	$u_1W_8^2/2$	$u_0/2$	IResult6

FIG. 4j

INTRA-ADD: DATA ELEMENTS OF IRESUT5, IRESULT6

$t_3W_8^1/2$	$t_2/2$	$t_1W_8^0/2$	$t_0/2$	IResult5
$u_3W_8^3/2$	$u_2/2$	$u_1W_8^2/2$	$u_0/2$	IResult6
$(u_2+u_3W_8^3)/2$	$(u_0+u_1W_8^2)/2$	$(t_2+t_3W_8^1)/2$	$(t_0+t_1W_8^0)/2$	F3-F0

FIG. 4k

INTRA-SUBTRACT: DATA ELEMENTS OF IRESUT5, IRESULT6

$t_3W_8^1/2$	$t_2/2$	$t_1W_8^0/2$	$t_0/2$	IResult5
$u_3W_8^3/2$	$u_2/2$	$u_1W_8^2/2$	$u_0/2$	IResult6
$(u_2-u_3W_8^3)/2$	$(u_0-u_1W_8^2)/2$	$(t_2-t_3W_8^1)/2$	$(t_0-t_1W_8^0)/2$	F7-F4

FIG. 4l

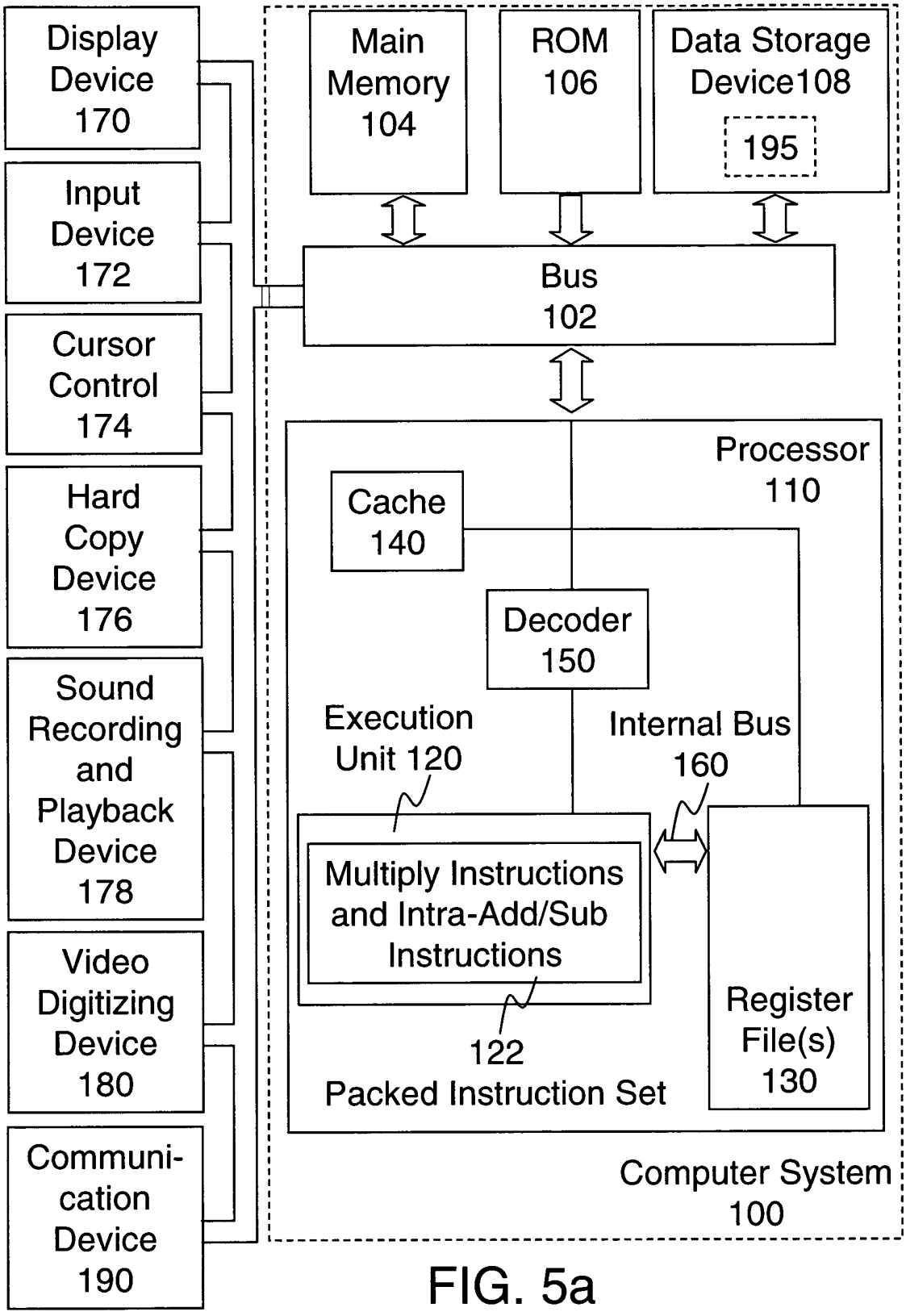

Display Device 170
Input Device 172
Cursor Control 174
Hard Copy Device 176
Sound Recording and Playback Device 178
Video Digitizing Device 180
Communi-cation Device 190
Main Memory 104
ROM 106
Data Storage Device108
195
Bus 102
Processor 110
Cache 140
Decoder 150
Execution Unit 120
Internal Bus 160
Multiply Instructions and Intra-Add/Sub Instructions
122
Packed Instruction Set
Register File(s) 130
Computer System 100

FIG. 5a

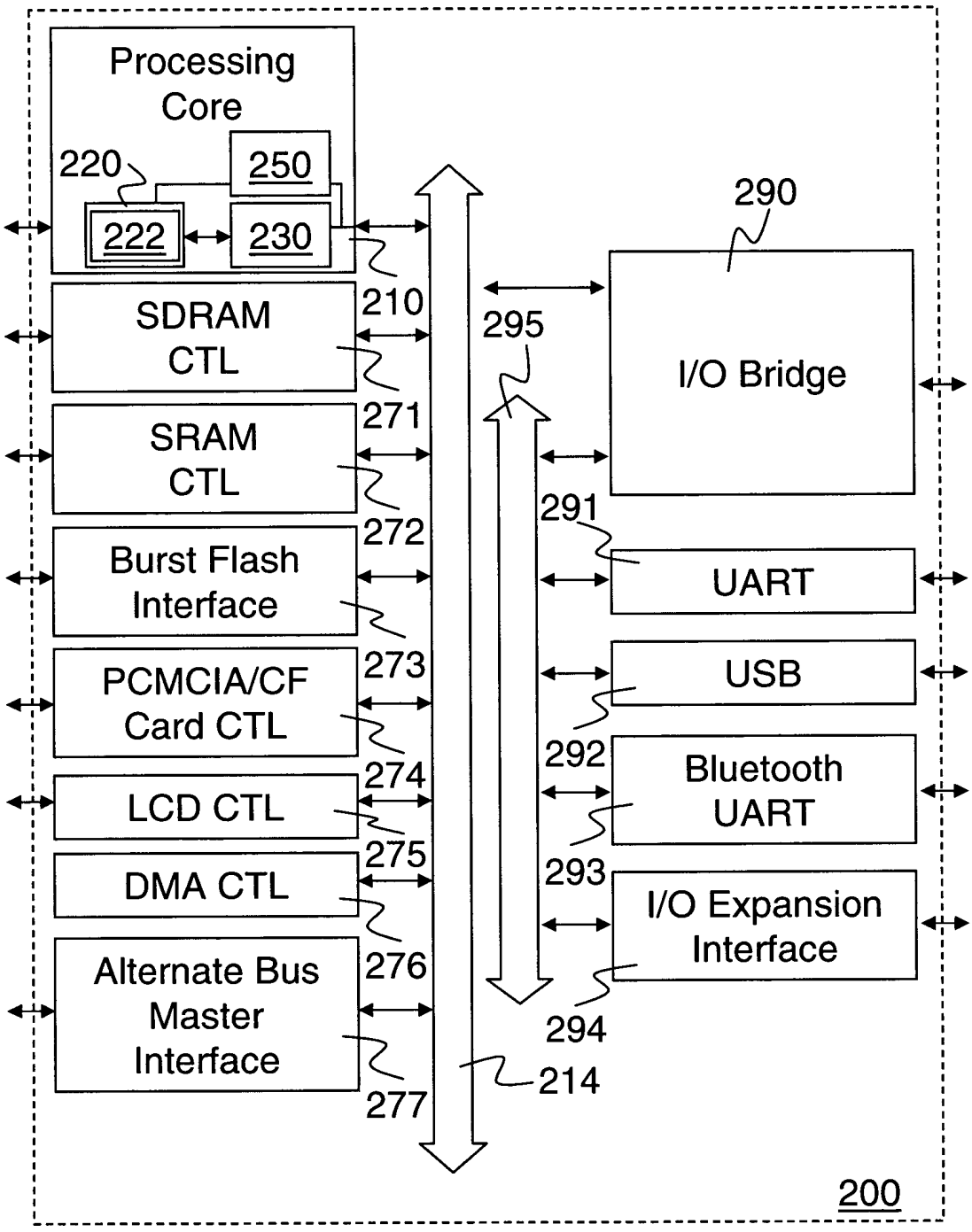

Processing Core
220
250
222
230
210
SDRAM CTL
271
SRAM CTL
272
Burst Flash Interface
273
PCMCIA/CF Card CTL
274
LCD CTL
275
DMA CTL
276
Alternate Bus Master Interface
277
214
295
290
I/O Bridge
291
UART
USB
292
Bluetooth UART
293
I/O Expansion Interface
294
200

FIG. 5b

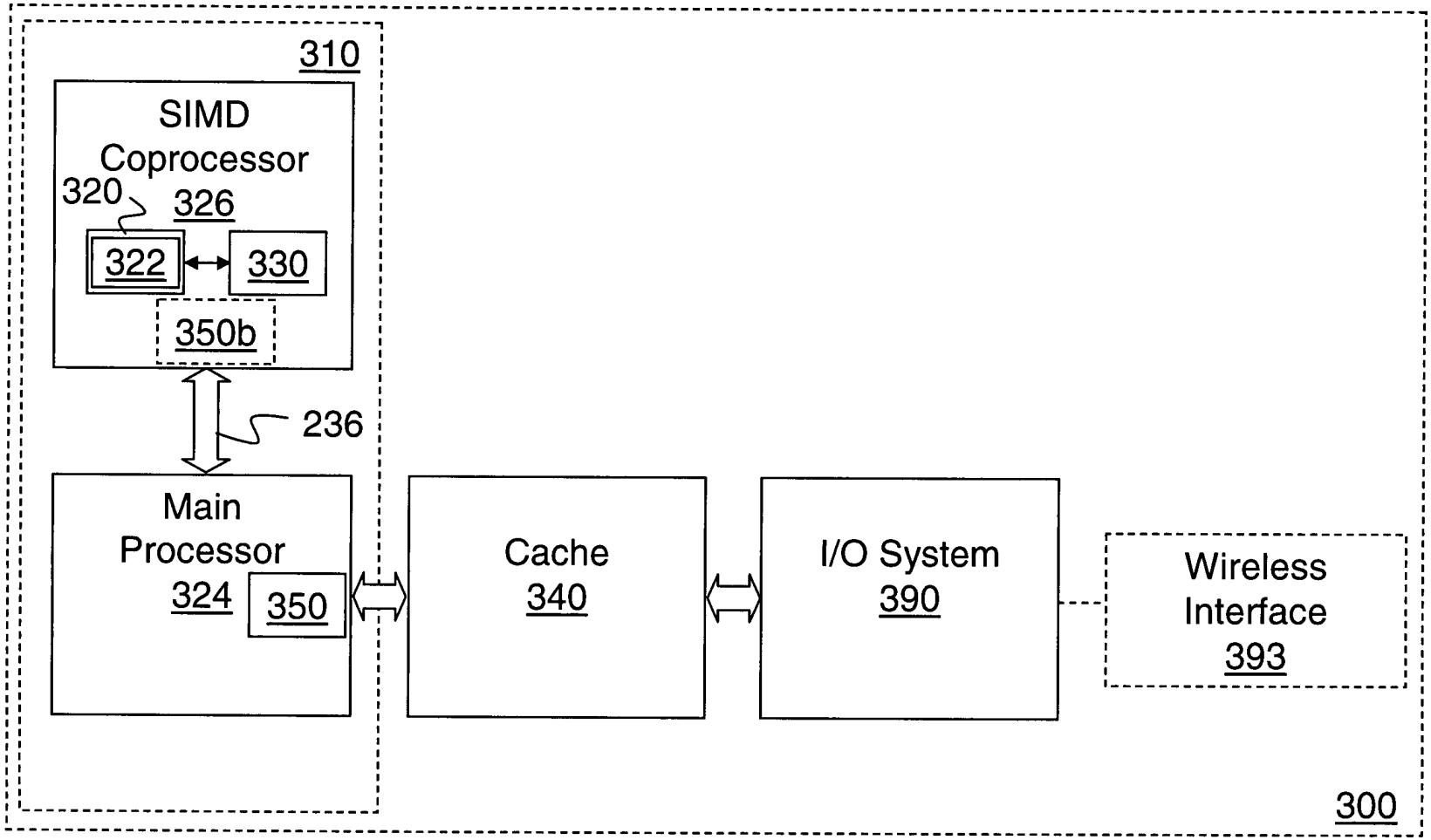

310
SIMD
Coprocessor
320
326
322
330
350b
236
Main
Processor
324
350
Cache
340
I/O System
390
Wireless
Interface
393
300

FIG. 5c

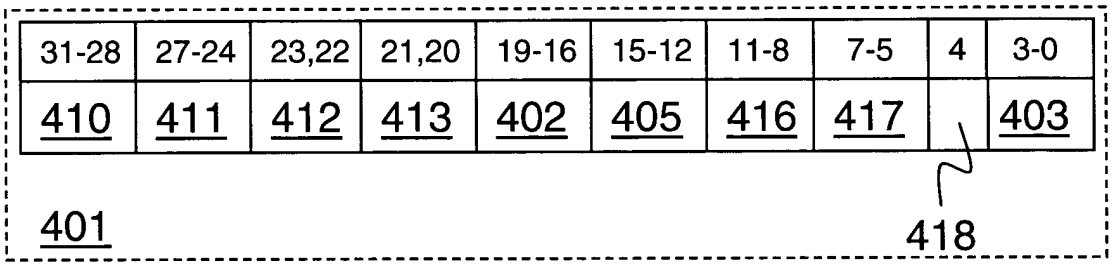


FIG. 6a

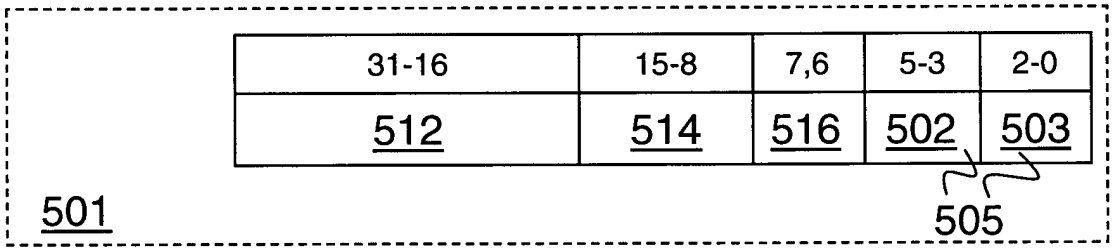


FIG. 6b

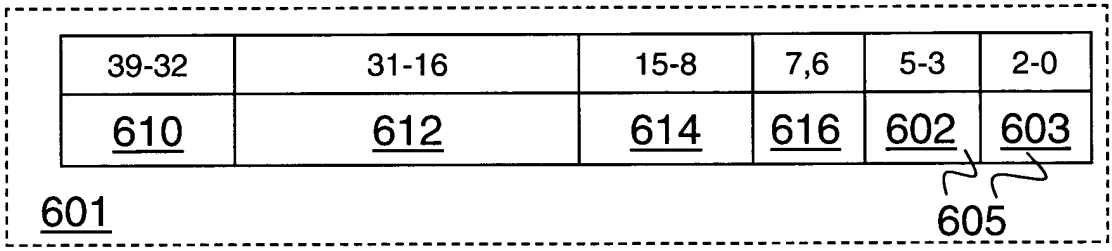


FIG. 6c

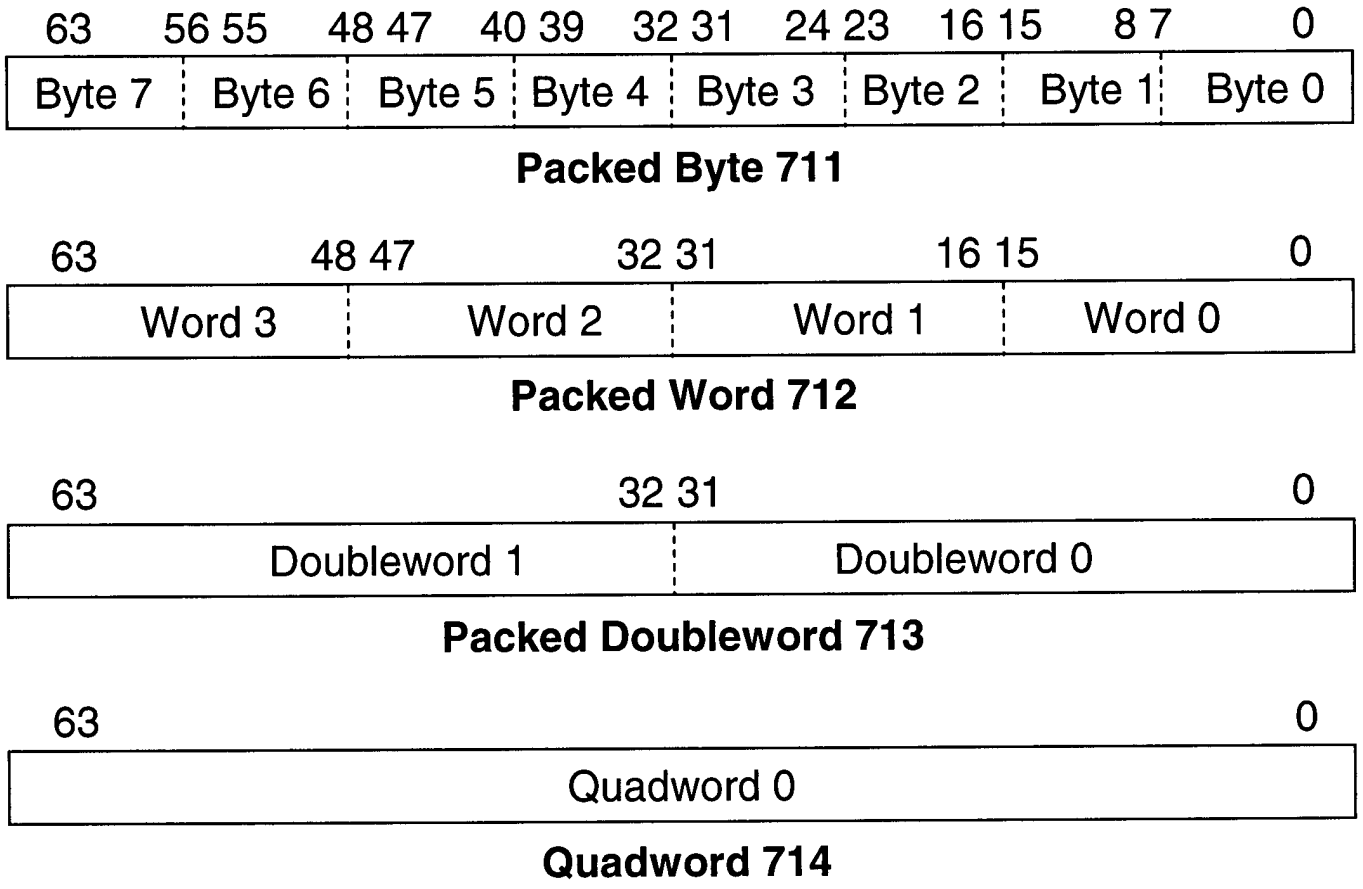

63 56 55 48 47 40 39 32 31 24 23 16 15 8 7 0
Byte 7
Byte 6
Byte 5
Byte 4
Byte 3
Byte 2
Byte 1
Byte 0
Packed Byte 711
63 48 47 32 31 16 15 0
Word 3
Word 2
Word 1
Word 0
Packed Word 712
63 32 31 0
Doubleword 1
Doubleword 0
Packed Doubleword 713
63 0
Quadword 0
Quadword 714

FIG. 7a

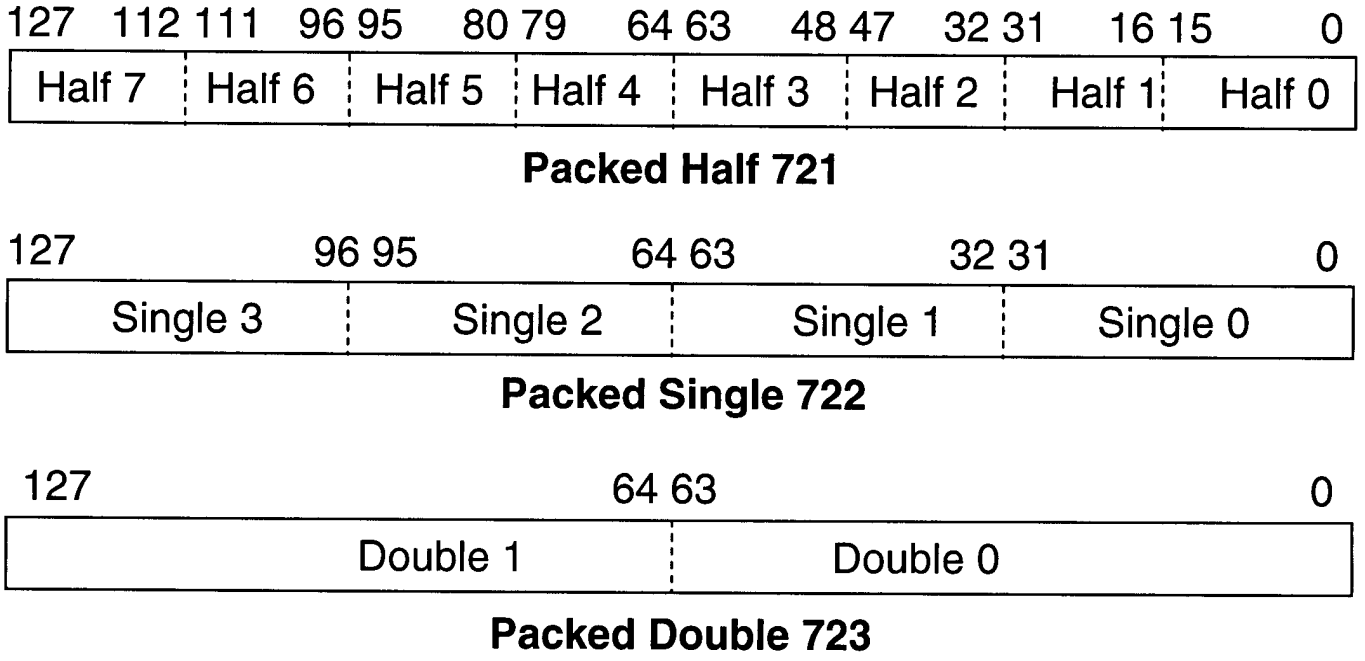

127 112 111 96 95 80 79 64 63 48 47 32 31 16 15 0
Half 7
Half 6
Half 5
Half 4
Half 3
Half 2
Half 1
Half 0
Packed Half 721
127 96 95 64 63 32 31 0
Single 3
Single 2
Single 1
Single 0
Packed Single 722
127 64 63 0
Double 1
Double 0
Packed Double 723

FIG. 7b

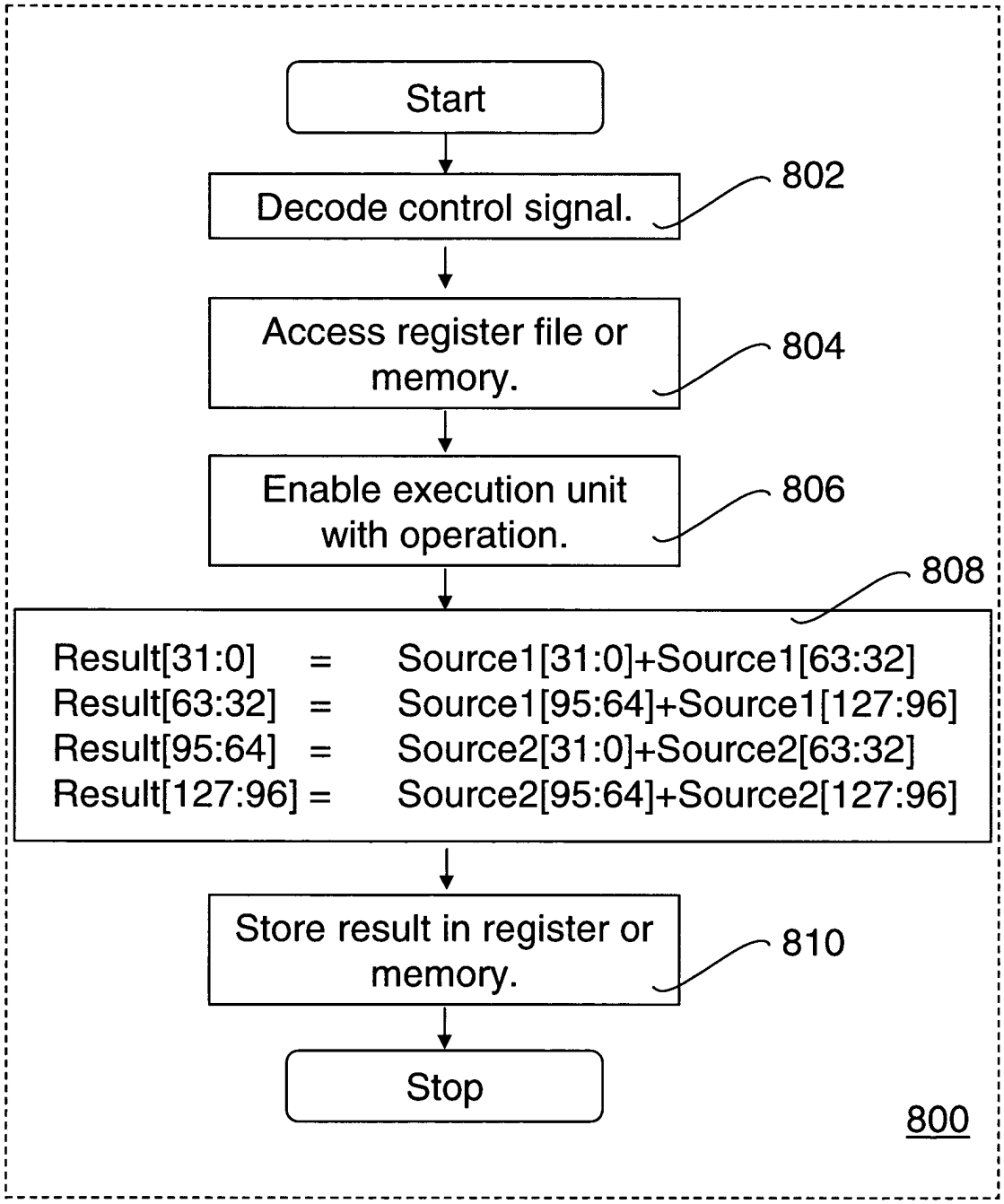

Start
Decode control signal.
802
Access register file or memory.
804
Enable execution unit with operation.
806
808
Result[31:0] = Source1[31:0]+Source1[63:32]
Result[63:32] = Source1[95:64]+Source1[127:96]
Result[95:64] = Source2[31:0]+Source2[63:32]
Result[127:96] = Source2[95:64]+Source2[127:96]
Store result in register or memory.
810
Stop
800

FIG. 8a

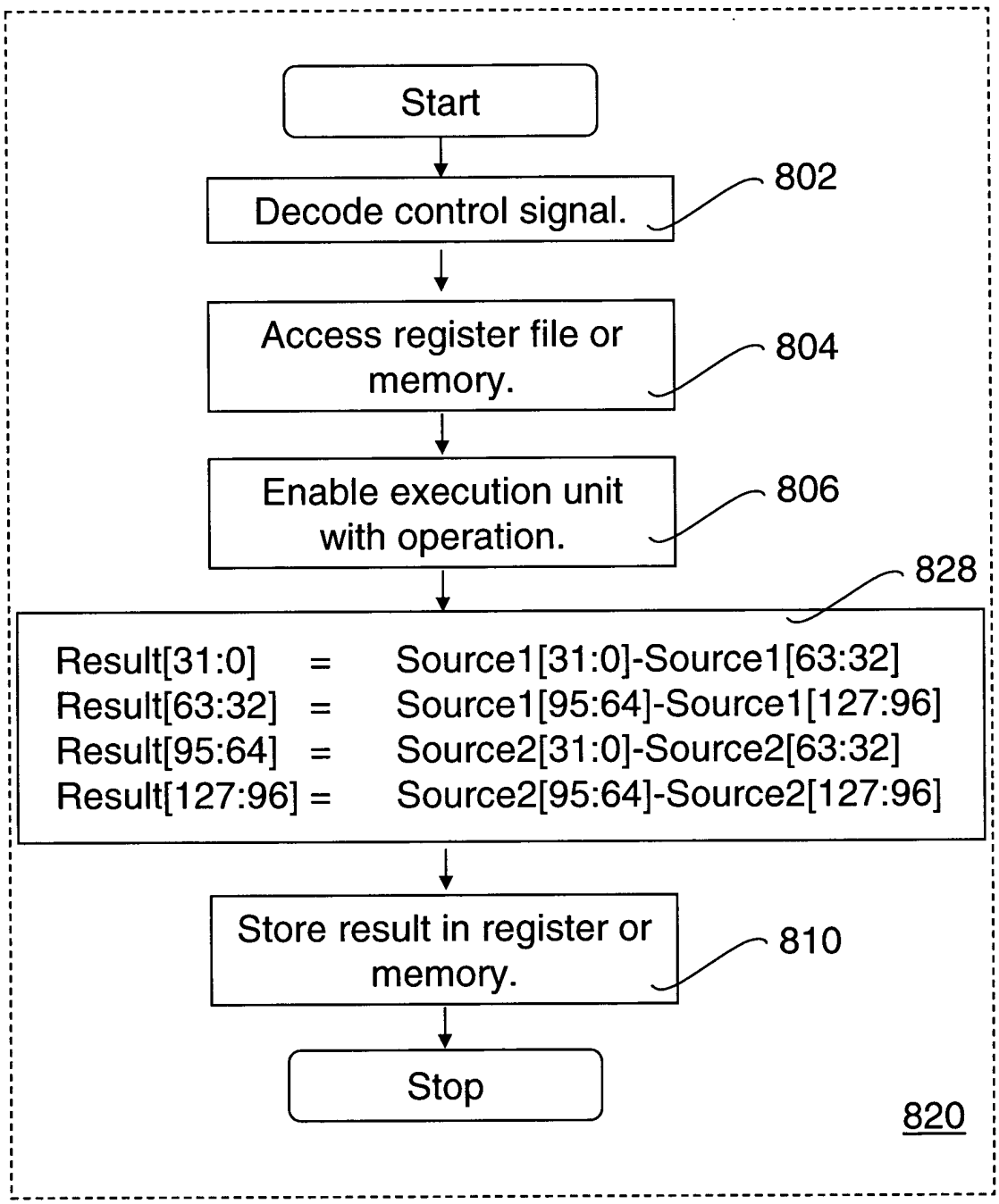

Start
Decode control signal.
802
Access register file or memory.
804
Enable execution unit with operation.
806
828
Result[31:0] = Source1[31:0]-Source1[63:32]
Result[63:32] = Source1[95:64]-Source1[127:96]
Result[95:64] = Source2[31:0]-Source2[63:32]
Result[127:96] = Source2[95:64]-Source2[127:96]
Store result in register or memory.
810
Stop
820

FIG. 8b

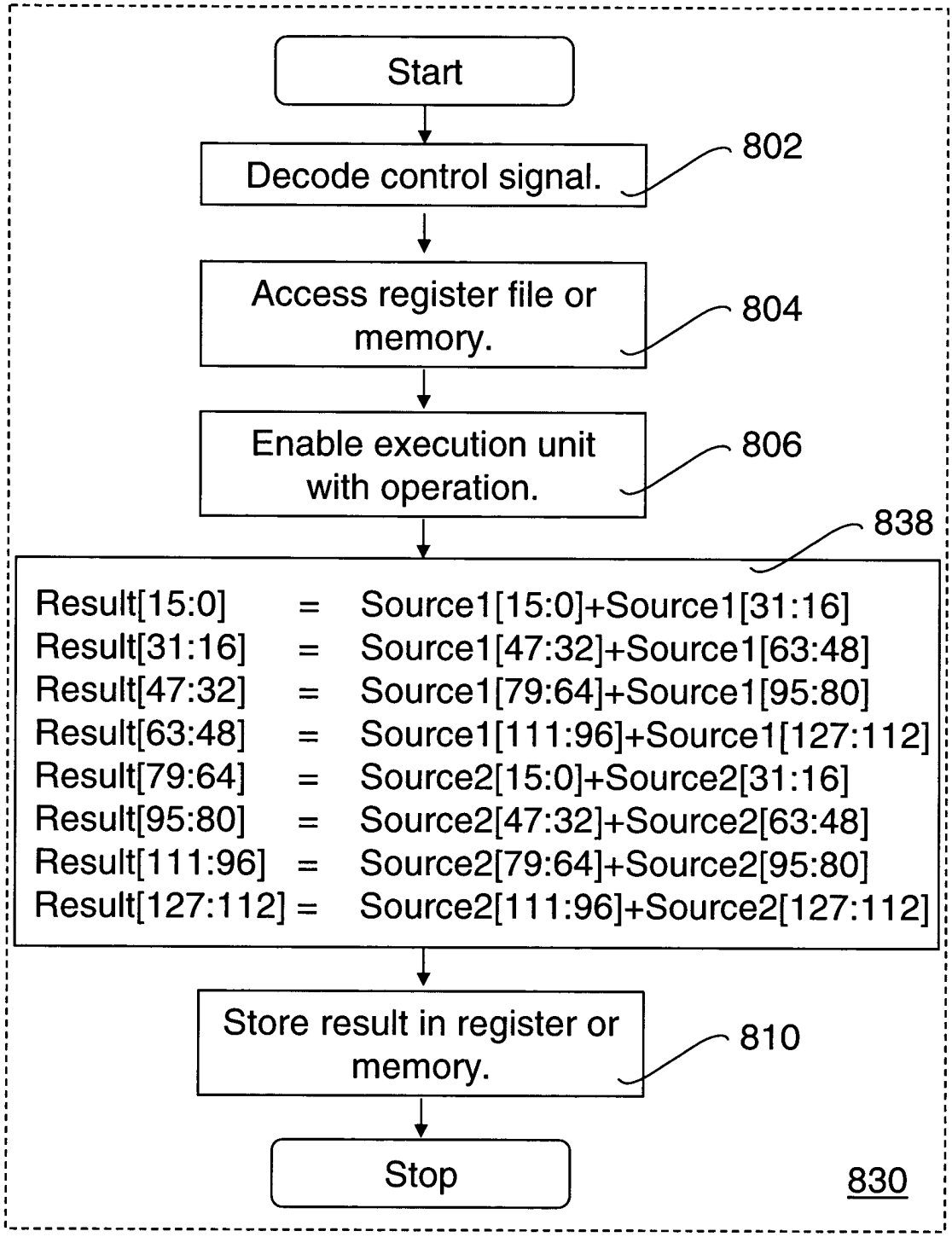

Start
Decode control signal.
802
Access register file or memory.
804
Enable execution unit with operation.
806
838
Result[15:0] = Source1[15:0]+Source1[31:16]
Result[31:16] = Source1[47:32]+Source1[63:48]
Result[47:32] = Source1[79:64]+Source1[95:80]
Result[63:48] = Source1[111:96]+Source1[127:112]
Result[79:64] = Source2[15:0]+Source2[31:16]
Result[95:80] = Source2[47:32]+Source2[63:48]
Result[111:96] = Source2[79:64]+Source2[95:80]
Result[127:112] = Source2[111:96]+Source2[127:112]
Store result in register or memory.
810
Stop
830

FIG. 8c

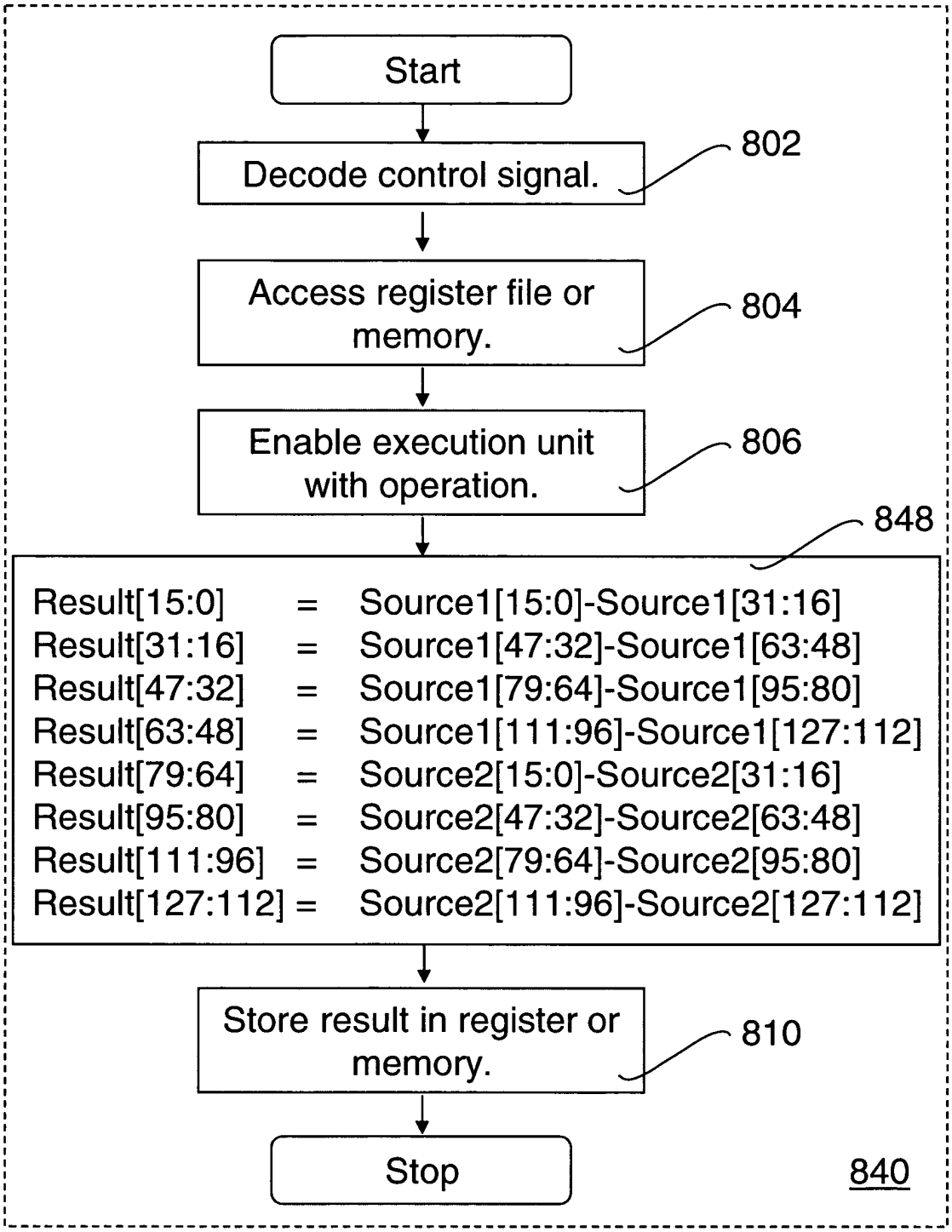

Start
Decode control signal.
802
Access register file or memory.
804
Enable execution unit with operation.
806
848
Result[15:0] = Source1[15:0]-Source1[31:16]
Result[31:16] = Source1[47:32]-Source1[63:48]
Result[47:32] = Source1[79:64]-Source1[95:80]
Result[63:48] = Source1[111:96]-Source1[127:112]
Result[79:64] = Source2[15:0]-Source2[31:16]
Result[95:80] = Source2[47:32]-Source2[63:48]
Result[111:96] = Source2[79:64]-Source2[95:80]
Result[127:112] = Source2[111:96]-Source2[127:112]
Store result in register or memory.
810
Stop
840

FIG. 8d

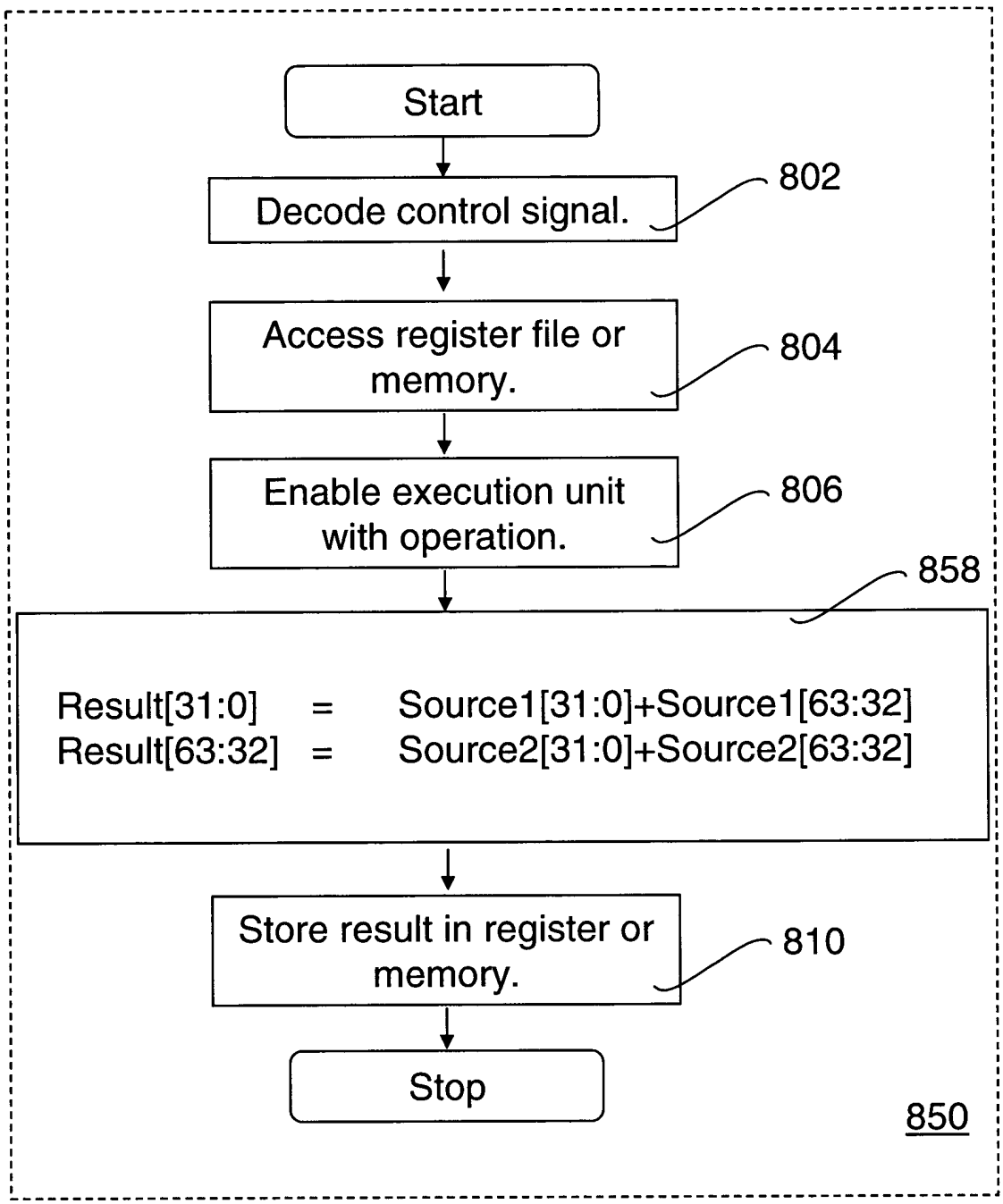

Start
Decode control signal.
802
Access register file or memory.
804
Enable execution unit with operation.
806
858
Result[31:0] = Source1[31:0]+Source1[63:32]
Result[63:32] = Source2[31:0]+Source2[63:32]
Store result in register or memory.
810
Stop
850

FIG. 8e

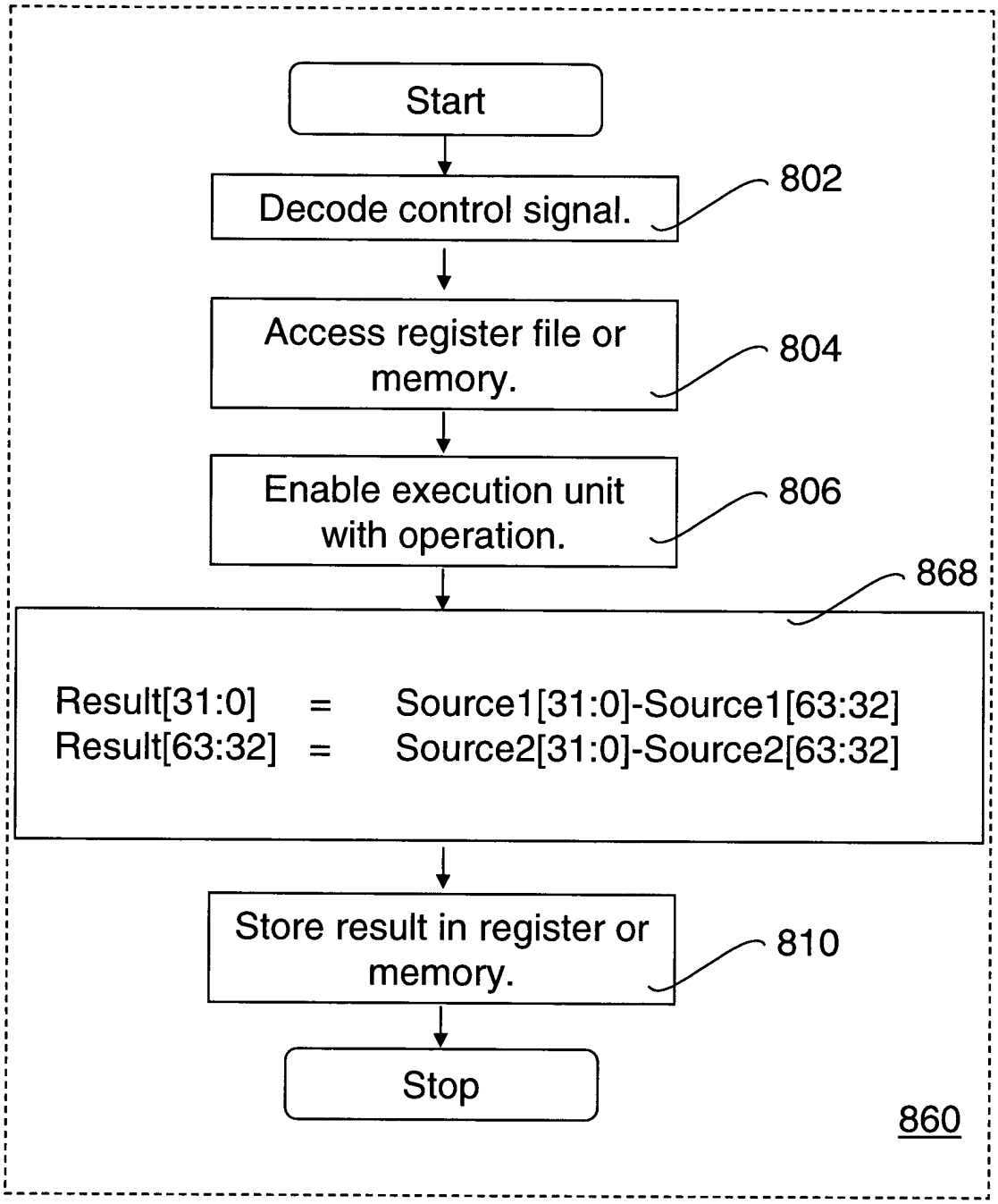

Start
Decode control signal.
802
Access register file or memory.
804
Enable execution unit with operation.
806
868
Result[31:0] = Source1[31:0]-Source1[63:32]
Result[63:32] = Source2[31:0]-Source2[63:32]
Store result in register or memory.
810
Stop
860

FIG. 8f

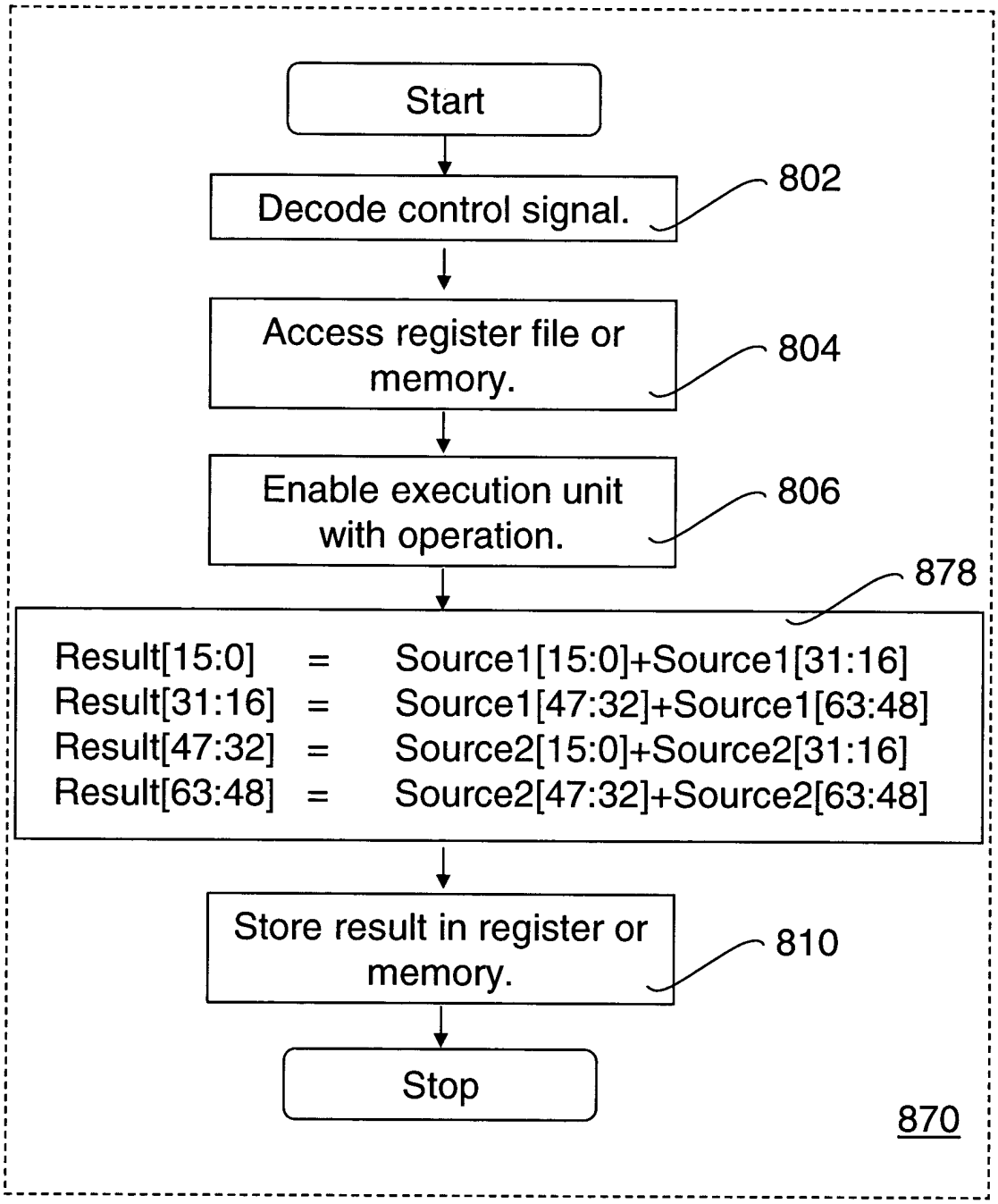

Start
Decode control signal.
802
Access register file or memory.
804
Enable execution unit with operation.
806
878
Result[15:0] = Source1[15:0]+Source1[31:16]
Result[31:16] = Source1[47:32]+Source1[63:48]
Result[47:32] = Source2[15:0]+Source2[31:16]
Result[63:48] = Source2[47:32]+Source2[63:48]
Store result in register or memory.
810
Stop
870

FIG. 8g

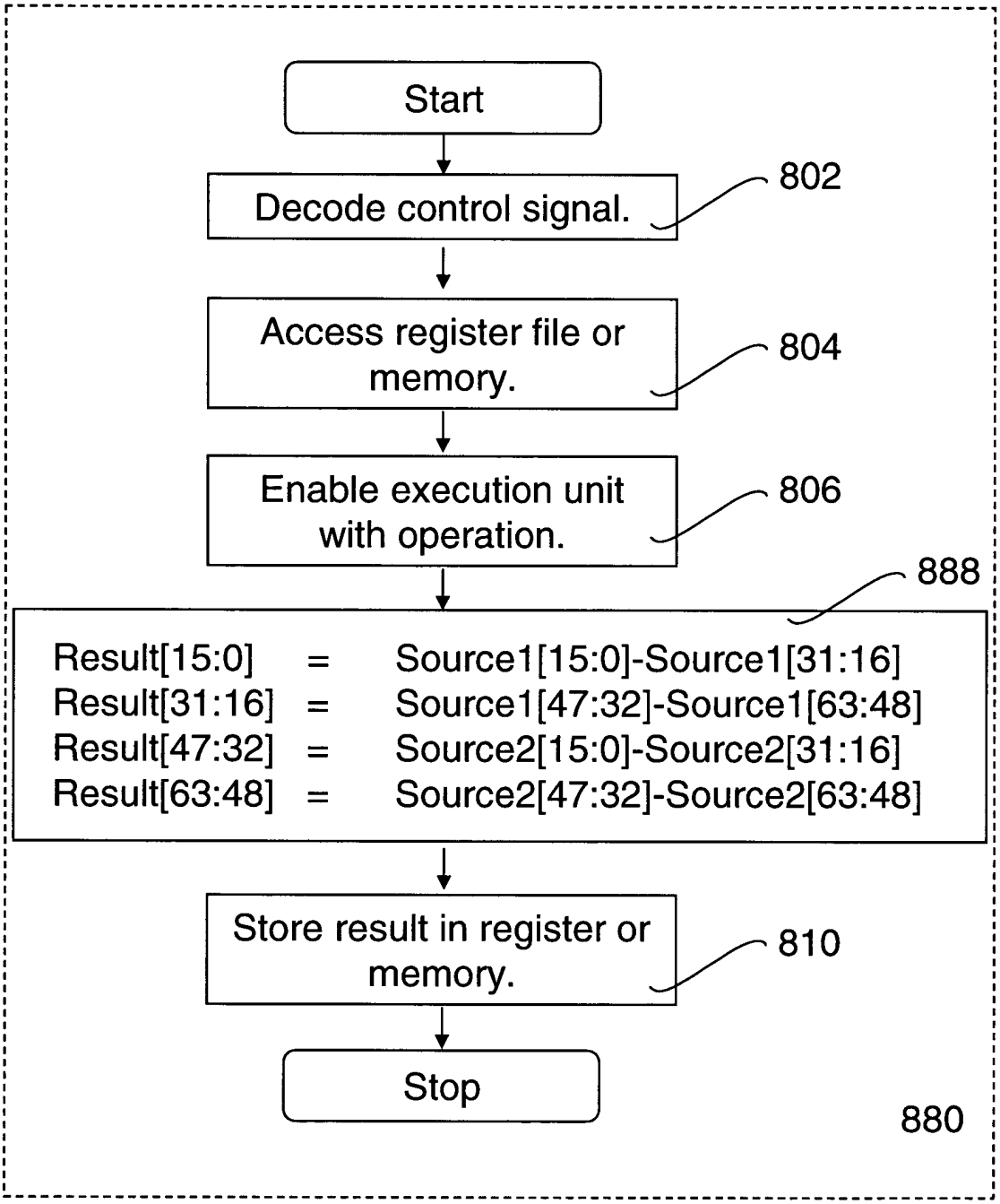

Start
Decode control signal.
802
Access register file or memory.
804
Enable execution unit with operation.
806
888
Result[15:0] = Source1[15:0]-Source1[31:16]
Result[31:16] = Source1[47:32]-Source1[63:48]
Result[47:32] = Source2[15:0]-Source2[31:16]
Result[63:48] = Source2[47:32]-Source2[63:48]
Store result in register or memory.
810
Stop
880

FIG. 8h

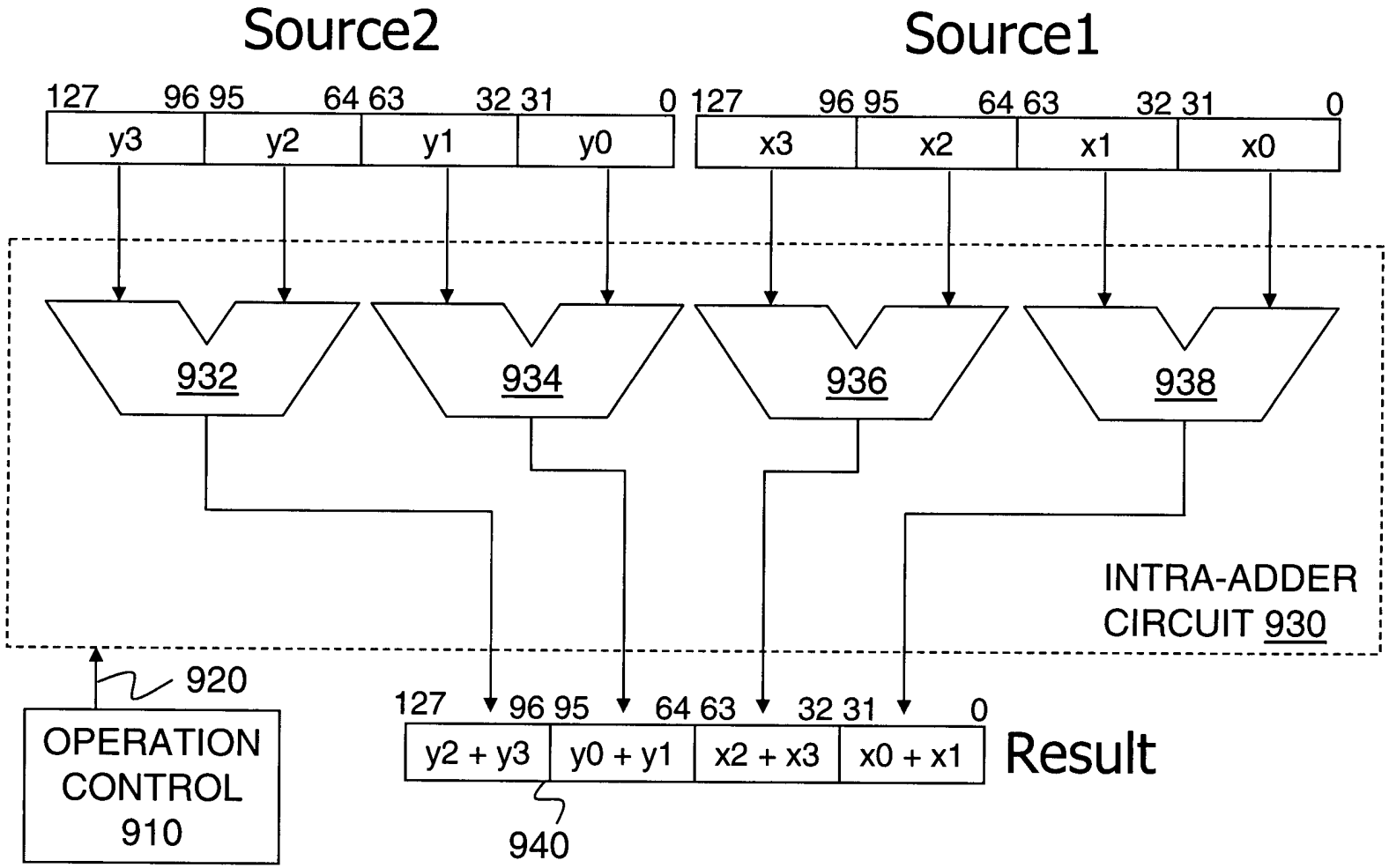

Source2
Source1
127
96 95
64 63
32 31
0
y3
y2
y1
y0
x3
x2
x1
x0
932
934
936
938
INTRA-ADDER
CIRCUIT 930
920
OPERATION
CONTROL
910
y2 + y3
y0 + y1
x2 + x3
x0 + x1
Result
940

FIG. 9a

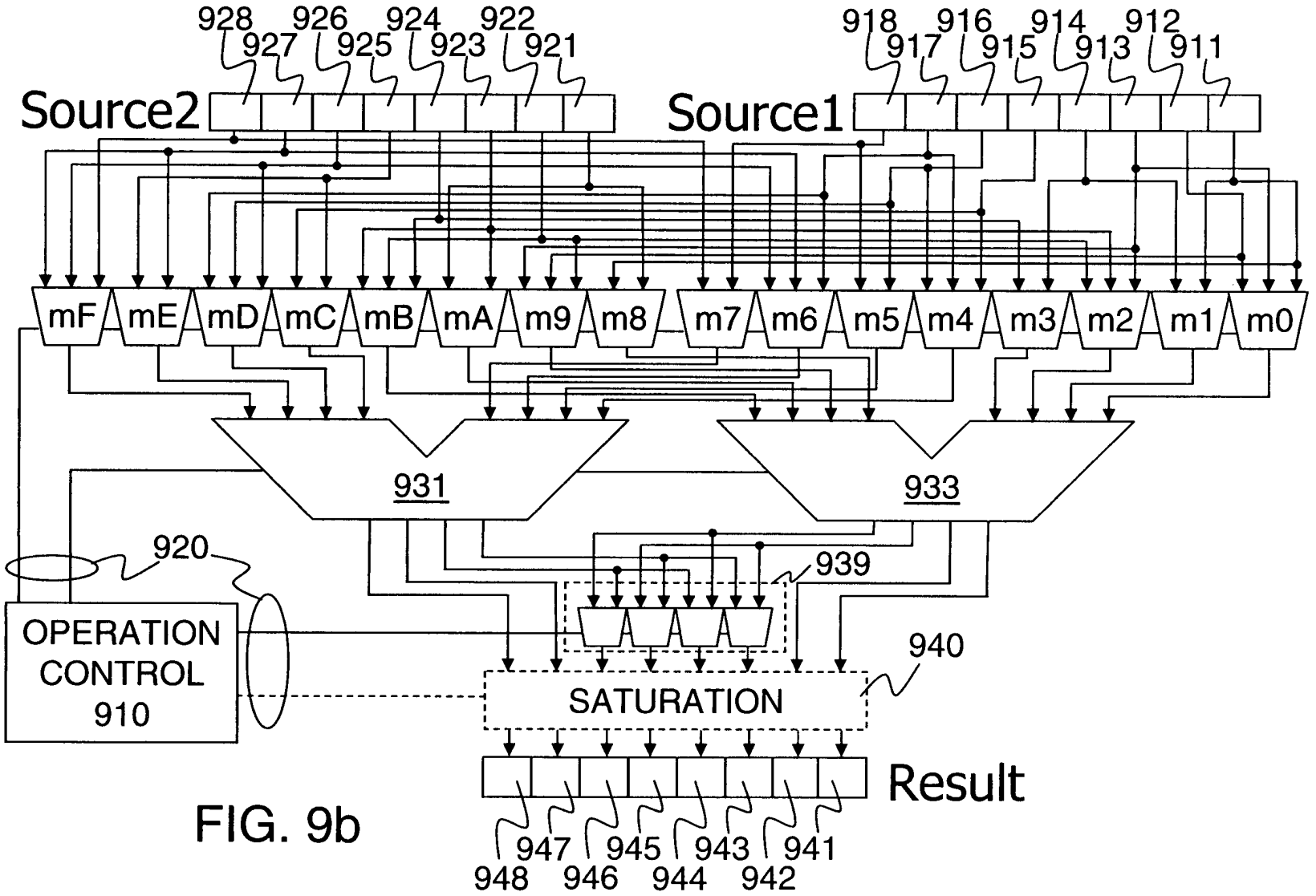

928
926
924
922
927
925
923
921
Source2
918
916
914
912
917
915
913
911
Source1
mF
mE
mD
mC
mB
mA
m9
m8
m7
m6
m5
m4
m3
m2
m1
m0
931
933
920
939
940
OPERATION
CONTROL
910
SATURATION
Result
947
945
943
941
948
946
944
942

FIG. 9b